The role of the Fermi level pinning in gate tunable graphene/semiconductor junctions: Barristor

Ferney A. Chaves* and David Jiménez
Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona, Campus UAB, 08193 Bellaterra (Barcelona), Spain.

*ferneyalveiro.chaves@uab.cat

Abstract

Graphene based transistors relying on a conventional structure cannot switch properly because of the absence of an energy gap in graphene. To overcome this limitation, a barristor device (Fig. 1) was proposed by Yang et al. [1], whose operation is based on the modulation of the graphene/semiconductor Schottky barrier by means of a top gate. ON-OFF current ratio up to 10^5 was demonstrated for a barristor. That large number is likely due to the realization of a clean interface with virtually no interface trapped charge that could spoil the barrier height tunability. However, it is indeed technologically relevant to know the impact that interface trapped charge might have on the barristor's electrostatics and carrier transport. For such a purpose we have developed a physics based model of the gate tunable graphene/semiconductor heterostructure where non-idealities such as Fermi Level Pinning (FLP) have been considered. Our study suggests that the barristor is a feasible graphene logic device achieving high enough on/off current ratio. When FLP dominates the barristor's electrostatics, the gate electrode cannot modulate the SBH anymore and rectification could be totally lost (Fig. 2). On the other hand, our model has revealed that the barristor exhibits changes of the threshold voltage induced by the drain-source voltage, similarly to the Drain Induced Barrier Lowering in short channel MOSFETs. It turns out that the barristor has to be biased at low V_{ds} to get a sufficient ON-OFF current ratio.

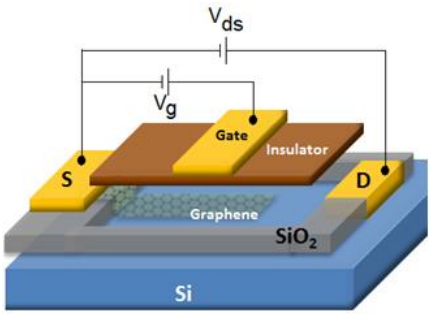

Fig. 1 Sketch of the barristor device.

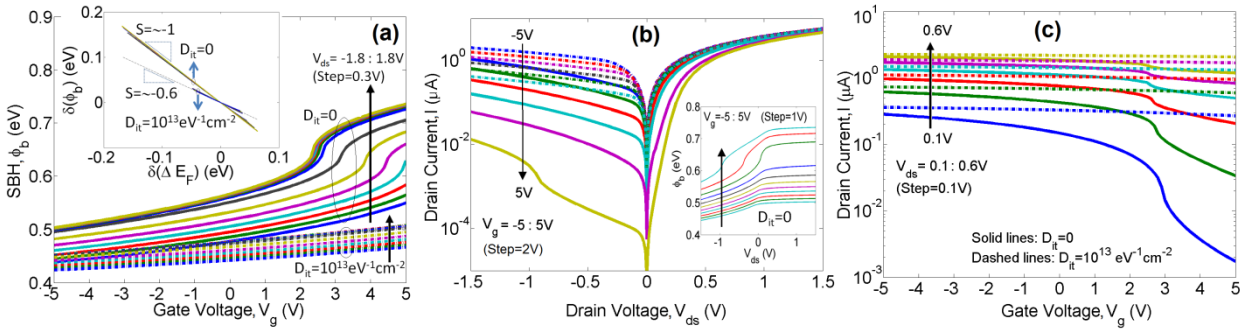

Fig. 2 Effect of the interface trapped charge on the SBH and current. Solid lines: without FLP and dashed lines: with FLP. (a) SBH curve for different values of V_{ds}. The inset shows the sensitivity of the SBH for a wide range of V_g and V_{ds}. The dashed line in the inset is a extrapolation of the simulated data. (b) Barristor's output characteristics. The inset displays the DIBL-like effect. (c) Barristor's transfer characteristics.

Acknowledgments:
The research leading to these results has received funding from the European Union Seventh Framework Programme under grant agreement n.604391 Graphene Flagship. The authors also acknowledge support from SAMSUNG within the Global Research Outreach Program and from Ministerio de Economía y Competitividad of Spain under the project TEC2015-67462- C2-1-R.

References

[1] Heejun Yang *et al., "*Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier", *Science* 336, 1140 (2012).
[2] Dhiraj Sinha and Ji Ung Lee, "Ideal Graphene/Silicon Schottky Junction Diode", Nano Lett. 14, 4660 (2014).
[3] Y. Taur, T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, May 2013.